REMARKS

The above Amendments and these Remarks are in reply to the Office Action mailed April 28, 2005.

The Examiner is requested to acknowledge the Information Disclosure Statement filed on May 5, 2005 by initialing the Form PTO-1449 and returning a copy of the initialed form to Applicants.

Currently, claims 1-57 are pending. Claims 1-24, 26-35, 37-45, 47, 48, 50, 52, 53 and 55-57 are amended. Claims 1 and 14 are amended to clarify that the behavior on which the categorizing of a set of non-volatile storage elements is based is a detected behavior. See, e.g., the specification, page 16, lines 4-7 and Fig. 5. No new matter is entered.

Applicants respectfully request reconsideration of the pending claims.

The claims have been amended in response to the rejection under 35 U.S.C. §112, second paragraph. Withdrawal of the rejection is therefore respectfully requested.

Regarding the objection under 37 C.F.R. §1.75, claim 17 has been amended based on claim 5 to avoid duplication with claim 16. Withdrawal of the objection is therefore respectfully requested.

Applicants acknowledge the indication that claims 4, 6, 7, 10, 15, 18 and 25-57 include allowable subject matter.

Claims 1-3, 5, 8, 9, 11-15, 17, and 19-24 have been rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,969,990 to Arase. Applicants respectfully traverse the rejection. Claim 1 sets forth a method for programming non-volatile memory in which a set of non-volatile storage elements are categorized into three or more groups based on a detected behavior of the non-volatile storage elements, and the non-volatile storage elements are programmed using a different programming condition for each group.

Arase provides a nonvolatile memory array where groups of memory transistors are connected to sub-bit lines, which in turn can be connected to a main bit line. For example, Figs. 2 and 5 provide NAND strings 1a and 1b which are connected to a sub-bit line SBLa. The sub-

bit line SBLa is connected to a main bit line MBLa via a connection transistor TG1a, and to a precharging line PCL via a connection transistor TG2a (col. 11, lines 6-13). The sub bit lines can be set at a programming prohibit potential at the time of a data programming operation (abstract). With this approach, the memory transistors are physically fixed in their respective groups by virtue of the NAND string or sub bit line with which they are associated.

Arase therefore fails to disclose or suggest categorizing a set of non-volatile storage elements into three or more groups based on a detected behavior of the non-volatile storage elements. Arase is not concerned with the detected behavior of non-volatile storage elements since the memory transistors are physically fixed in their respective groups at the time of manufacture, regardless of any detected behavior. Applicants' approach allows the programming process to be adapted based on the behavior of the storage elements (specification, page 4, lines 9-11, page 16, lines 9-18). In particular, the storage elements are programmed using a different programming condition for each group. This approach can result in various benefits including a reduced threshold voltage distribution (page 10, lines 14-18).

Regarding the Examiner's assertion that the controlling circuit 20 (Arase, Fig. 1) causes a categorizing of the memory transistors into three or more groups, Applicants note that there is no action performed by the controlling circuit which can be considered to constitute categorizing. Instead, as mentioned, the transistors are only physically arranged in different groups at the time of manufacture. Arase provides no disclosure or suggestion of categorizing storage elements, that is, placing storage elements into categories. While claims can be interpreted during examination using the broadest reasonable interpretation, the interpretation must also be consistent with the interpretation that those skilled in the art would reach. In re Cortright, 165 F.3d 1353, 1359, 49 USPQ2d 1464, 1468 (Fed. Cir. 1999). Applicants respectfully submit that the Examiner's interpretation of "categorizing" does not meet this requirement.

Accordingly, independent claims 1 and 14 are clearly patentable over the cited reference. Moreover, the dependent claims recite further patentable features. For example, claims 5 and 16 set forth that the categorizing includes determining programmability of the non-volatile storage elements relative to each other, each group including non-volatile storage elements with similar

programmability. Arase simply fails to disclose or suggest such categorizing of storage elements into groups based on a determined programmability. Instead, the memory transistors of Arase are physically arranged in different groups at the time of manufacture regardless of any determined programmability. Furthermore, Applicants note that the Office Action fails to specify how the features of claims 5 and 16, among other rejected dependent claims, are met by the cited reference.

Regarding claims 8 and 20, these claims set forth that initial programming is applied to storage elements prior to programming using a different programming condition, and the categorizing is based on the initial programming. The Office Action indicates that these features are shown in Figs. 5 and 6 of Arase. However, these figures provide no disclosure or suggestion of categorizing storage elements based on initial programming which is applied to the storage elements. Instead, Fig. 5 provides a memory layout, while Fig. 6 provides an associated timing chart. In particular, Fig. 6 indicates how two programming/verifying operations are carried out in time periods t1-t4 and t4-t7 (col. 13, lines 3-12). There is no mention of categorizing storage elements based on initial programming. Instead, the memory transistors are only physically arranged in different groups at the time of manufacture regardless of any initial programming.

Regarding claims 11 and 21, which depend on claims 8 and 20, respectively, these claims set forth that the applying of the initial programming is performed until at least one non-volatile storage element reaches a target threshold value, and the categorizing is performed for non-volatile storage elements that did not yet reach the target threshold value. Again, Applicants respectfully note that the Office Action fails to specify how the features of these claims are met by the cited reference. Arase simply provides no disclosure or suggestion of categorizing non-volatile storage elements that did not yet reach a target threshold value.

Based on the above amendments and these remarks, reconsideration of the claims is respectfully requested.

The Examiner's prompt attention to this matter is greatly appreciated. Should further questions remain, the Examiner is invited to contact the undersigned attorney by telephone.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 501826 for any matter in connection with this response, including any fee for extension of time, which may be required.

Respectfully submitted,

Date: 7-28-05 By: Ralph F. Hoppin

Ralph F. Hoppin
Reg. No. 38,494

VIERRA MAGEN MARCUS HARMON & DENIRO LLP
685 Market Street, Suite 540
San Francisco, California 94105-4206
Telephone: (415) 369-9660
Facsimile: (415) 369-9665